CLAIMS

What is claimed is:

1. A semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side and a side extending transversely therebetween;

a plurality of bond pads over the active surface in a first arrangement; and

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion and including a first plurality of electrical contacts on the first side of the first portion connected to the bond pads of the plurality and communicating through conductive traces with at least a second plurality of electrical contacts in a second arrangement different from the first arrangement on the second side of the second portion;

wherein the first portion of the interposer substrate extends and is secured over the active surface of the first semiconductor die, the second portion is secured over the back side thereof and the spacer portion extends over the side thereof.

2. The semiconductor die assembly of claim 1, further including discrete conductive elements disposed over the contacts of the second plurality and projecting transversely therefrom.

3. The semiconductor die assembly of claim 2, wherein the second arrangement comprises a two-dimensional array.

4. The semiconductor die assembly of claim 1, further including a third plurality of electrical contacts on the second side of the first portion in a third arrangement in communication with the first plurality of electrical contacts through conductive traces.

5. The semiconductor die assembly of claim 4, wherein the third arrangement is a mirror image of the second arrangement.

6. The semiconductor die assembly of claim 5, wherein the second arrangement comprises a two-dimensional array.

7. The semiconductor die assembly of claim 4, further including discrete conductive elements disposed over the contacts of the third plurality and projecting transversely to the active surface of the first die.

8. The semiconductor die assembly of claim 4, further including discrete conductive elements disposed over the contacts of one of the second plurality and the third plurality and projecting transversely therefrom.

9. The semiconductor die assembly of claim 8, further including a second die disposed over the first die and in electrical communication with the first die through another of the second plurality and the third plurality of contacts.

10. The semiconductor die assembly of claim 9, wherein the second die includes discrete conductive elements projecting transversely therefrom, by which the electrical communication with the first die is effected.

11. The semiconductor die assembly of claim 10, wherein the second die is configured substantially identical to the first die.

12. The semiconductor die assembly of claim 1, further including an underfill material disposed between the active surface of the first die and the first side of the first portion of the interposer substrate.

13. The semiconductor die assembly of claim 1, further comprising an adhesive layer over the back side of the first die securing the second portion of the interposer thereto.

14. The semiconductor die assembly of claim 1, wherein the first and second portions of the interposer substrate are each of a length and width substantially corresponding to a length and width of the first die.

15. A semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side, a side extending transversely therebetween and a plurality of bond pads over the active surface in a first arrangement;

a second semiconductor die having an active surface, an opposing back side, a side extending transversely therebetween and a plurality of bond pads over the active surface in a second arrangement; and

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a first spacer portion and including:

a first plurality of electrical contacts on the first side of the first portion connected to the bond pads of the plurality of the first semiconductor die;

a second plurality of electrical contacts on the second side of the first portion connected to the bond pads of the plurality of the second semiconductor die;

a third plurality of electrical contacts on at least one of the first and second sides of the second portion and in communication through conductive traces with the first and second plurality of contacts, the third plurality of contacts being in a third arrangement differing from the first and second arrangements;

wherein the first portion of the interposer substrate extends and is secured between the first and second semiconductor dice, the second portion is secured over the back side of one of the first and second semiconductor dice with the contacts of the third plurality accessible and the spacer portion extends over the side of the one of the first and second semiconductor dice to which the second portion is secured.

16. The semiconductor die assembly of claim 15, wherein the first and second arrangements are identical.

17. The semiconductor die assembly of claim 15, wherein the second arrangement comprises a mirror image of the second arrangement.

18. The semiconductor die assembly of claim 15, wherein the third plurality of electrical contacts is exposed on both the first and second sides of the second portion.

19. The semiconductor die assembly of claim 18, wherein the electrical contacts of the third plurality comprise conductive material-filled vias extending from the first side to the second side of the second portion of the interposer substrate.

20. The semiconductor die assembly of claim 18, further comprising discrete conductive elements disposed on and projecting transversely from the accessible contacts of the third plurality.

21. The semiconductor die assembly of claim 15, further comprising discrete conductive elements disposed on and projecting transversely from the accessible contacts of the third plurality.

22. The semiconductor die assembly of claim 15, wherein the third arrangement comprises a two dimensional array.

23. The semiconductor die assembly of claim 15, wherein the second portion of the interposer substrate comprises two adjacent second portions separated by a second spacer portion, one second portion is secured over the back side of one of the first and second semiconductor dice, the other second portion is secured over the back side of another of the first and second semiconductor dice, the first space portion extends over a side of the one of the semiconductor dice and the second spacer portion extends over the side of the another of the semiconductor dice.

24. The semiconductor die assembly of claim 23, wherein the third plurality of electrical contacts is disposed on one of the two second portions.

25. The semiconductor die assembly of claim 24, further including discrete conductive elements disposed on the contacts of the third plurality and projecting transversely therefrom.

26. The semiconductor die assembly of claim 24, further comprising a fourth plurality of contacts disposed on another of the two second portions and in communication with electrical contacts of at least one of the first and second plurality through conductive traces.

27. The semiconductor die assembly of claim 26, further including discrete conductive elements disposed on the contacts of either the third plurality or the fourth plurality and projecting transversely therefrom.

28. The semiconductor die assembly of claim 27, further including at least another semiconductor die disposed over the semiconductor die assembly and in electrical communication with the semiconductor die assembly through contacts of either the third or fourth plurality having no discrete conductive elements disposed thereon.

29. The semiconductor die assembly of claim 28, wherein the at least another semiconductor die includes discrete conductive elements projecting transversely therefrom, by which the electrical communication with the semiconductor die assembly is effected.

30. The semiconductor die assembly of claim 29, wherein the at least another semiconductor die assembly comprises another multiple-die assembly.

31. The semiconductor die assembly of claim 15, further including an underfill material respectively disposed between the active surfaces of the first semiconductor die and the second semiconductor die and the first and second sides of the first portion of the interposer substrate.

32. The semiconductor die assembly of claim 15, further comprising an adhesive layer over the back side of the one of the first semiconductor die and the second semiconductor die having the second portion of the interposer secured thereto.

33. The semiconductor die assembly of claim 15, wherein the first and second portions of the interposer substrate are each of a length and width substantially corresponding to a length and width of at least one the first semiconductor die and the second semiconductor die.

34. A semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side and a side extending transversely therebetween;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion, the first portion disposed over the active surface of the first semiconductor die and the second portion disposed over the back side thereof with the spacer portion over the side thereof, the interposer substrate further including conductive traces electrically connected to the first die and extending between the first portion and the second portion to an array of discrete conductive elements projecting transversely from the back side.

35. A semiconductor die assembly comprising:

first and second semiconductor dice having mutually facing active surfaces;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion, the first portion being disposed between the first and second semiconductor dice and the second portion being secured over a back side of one of the first and second semiconductor dice with the spacer portion over a side of the semiconductor die over which the second portion is secured, the interposer further including conductive traces electrically connected to the first and second semiconductor dice and extending between the first portion and the second portion to an array of discrete conductive elements projecting from the back side of the semiconductor die to which the second portion is secured.

36. An interposer substrate for use with to at least one semiconductor die having an active surface and a back side, the interposer substrate comprising:

a flexible dielectric substrate having a first portion and a adjacent second portion separated by a spacer portion; and

a first plurality of electrical contacts on a first side of the first portion arranged to mate with bond pads of a first selected semiconductor die and connected to a second plurality of electrical contacts on a side of a second portion of the interposer substrate through conductive traces, the second plurality of electrical contacts being in a different arrangement than the first.

37. The interposer substrate of claim 36, further comprising a third plurality of electrical contacts on a second side of the first portion, arranged to mate with bond pads of a second semiconductor die and electrically connected through conductive traces to contacts of the second plurality.

38. The interposer substrate of claim 37, further comprising a fourth plurality of electrical contacts on another side of the second portion electrically connected to the electrical contacts of the first and third pluralities through conductive traces.

39. The interposer substrate of claim 38, wherein the second and fourth pluralities of electrical contacts are connected.

40. The interposer substrate of claim 39, wherein the second and fourth contacts lie at opposing ends of conductive vias extending transversely through the second portion.

41. The interposer substrate of claim 38, wherein the second and fourth pluralities of contacts comprise two-dimensional arrays.

42. The interposer substrate of claim 41 wherein the two-dimensional arrays comprise mirror images.

43. A method for fabricating a semiconductor die assembly, the method comprising:

providing a first semiconductor die having a first surface which oppositely faces a second surface thereof and having a side between the first and second surfaces; and

attaching one side of a first portion of a substrate to the first surface, wrapping the substrate around the side and attaching a second portion of the substrate to the second surface of said at least one semiconductor die to substantially cover the first and second surfaces.

44. The method of claim 43, further comprises disposing discrete conductive elements on the second portion of the substrate.

45. The method of claim 43, further comprising:

providing a second semiconductor die having a first surface which oppositely faces a second surface thereof and having a side between the first and second surfaces thereof;

attaching another side of the first portion of the substrate to first surface of the second die.

46. The method of claim 45, wherein the attaching the first portion of the substrate to the first and second semiconductor dice is effected prior to the wrapping of the substrate.

47. The method of claim 46, further comprises disposing discrete conductive elements on the second portion of the substrate.

48. The method of claim 47, further comprising conductively connecting the semiconductor die assembly to a carrier substrate using the discrete conductive elements.

49. The method of claim 43, further comprising conductively connecting the semiconductor die assembly to a carrier substrate using the discrete conductive elements.

50. An electronic assembly, comprising:

a semiconductor die assembly comprising:

a first semiconductor die having an active surface, an opposing back side and a side extending transversely therebetween;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion, the first portion disposed over the active surface of the first semiconductor die and the second portion disposed over the back side thereof with the spacer portion over the side thereof, the interposer substrate further including conductive traces electrically connected to the first die and extending between the first portion and the second portion to an array of discrete conductive elements projecting transversely from the back side; and

a higher level packaging structure connected to the semiconductor die assembly through the discrete conductive elements.

51. The electronic assembly of claim 50, wherein the higher level packaging structure comprises a computer.

52. An electronic assembly, comprising:

a semiconductor die assembly comprising:

first and second semiconductor dice having mutually facing active surfaces;

a flexible dielectric interposer substrate having first and second opposing sides and first and second adjacent portions separated by a spacer portion, the first portion being disposed between the first and second semiconductor dice and the second portion being secured over a back side of one of the first and second semiconductor dice with the spacer portion over a side of the semiconductor die over which the second portion is secured, the interposer further including conductive traces electrically connected to the first and second semiconductor dice and extending between the first portion and the second portion to an array of discrete conductive elements projecting from the back side of the semiconductor die to which the second portion is secured; and

a higher level packaging structure connected to the semiconductor die assembly through the discrete conductive elements.

53. The electronic assembly of claim 52, wherein the higher level packaging structure comprises a computer.